Atri Bhattacharyya

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Morges, Vaud
Switzerland

INTERESTS

- Micro-architectural security and design
- Datacenter architectures

EDUCATION

Doctoral assistant, Computer Science, 2^{nd} year 2018 onwards
Ecole Polytechnique Federale de Lausanne, Switzerland

MS in Computer Science 2016 - 2018
Ecole Polytechnique Federale de Lausanne, Switzerland
Current GPA: 5.73/6 (equivalent to 3.73/4)

BT in Electrical Eng with major in Computer Science and Eng 2011 - 2016
Indian Institute of Technology Kanpur, India
GPA: 9.1/10 (equivalent to 3.64/4)

RESEARCH

SMoTherSpectre: Exploiting speculative execution through port contention
Worked with **Prof. Mathias Payer** on a speculative-execution attack using port contention as a side-channel. Allows leakage of plaintext information from OpenSSL.

MS project Feb 2018 - July 2018
Laboratoire d'architecture des processeurs (LAP)
Worked with **Prof. Paolo Ienne** on optimizing load-store queue design for dynamically-scheduled elastic circuits generated by high-level synthesis. By exploiting temporal-ordering between memory operations, my optimization reduces the estimated hardware cost for LSQs by as much as 93%.

MS Research Scholar Sept 2016 - August 2017
Parallel Systems Architecture Lab, EPFL, Switzerland
Worked with **Prof. Babak Falsafi** on various projects.

- Investigated the impact of speculative store retirement by extending the memory-ordering capabilities of a full-system cycle-accurate simulator (Flexus).
- Designed a netork-on-chip(NOC) for practical Scale-out-processors and investigated other aspects of the design to enable sharing on-chip resources.

MITACS Globalinks Research Intern May 2015 - July 2015
University of Alberta, Edmonton, Canada
Worked with **Prof. Duncan Elliott** to develop an experimental, open-source cube satellite, ExAlta-1, at the University of Alberta.

- Implemented the data-acquisition framework for the primary payloads: multi-Needle Langmuir Probe (mNLP) and Digital Fluxgate Magnetometer(DFGM).
- Developed the link-layer drivers for Cubesat Space Protocol(CSP) networking.

INDUSTRY EXPERIENCE

Research Assistant August 2017 - Present
Oracle Labs, Zurich, Switzerland
Developed a DPDK-based multi-user capable userspace-networking framework capable of saturating 10Gbit/s interfaces with a single core while providing the benefits of in-kernel networking: isolation, flexibility and security.

- Integrated the framework with a network-processing bound DDoS detection pipeline to increase its maximum throughput by around 15x.

UnnaTI Embedded Software Intern May 2014 - July 2014
Texas Instruments, Bangalore, India
Developed a profiler to show cycle-wise timing of C/assembly level instruction execution on an embedded platform to enable rapid profiling and benchmarking to:

- Augment and verify manual benchmarking results in less than 20% of the time.
- Benchmark and optimize TIs low-power MCU software framework and FreeRTOS on Cortex-M0+ processor. Achieved more than 50% improvement for certain OS benchmarks.

PUBLICATIONS

- *Shrink It and Shred It! Minimize the Use of LSQs in Dataflow Designs*, Josipovic et al., In: International Conference on Field-Programmable Technology, 2019.
- *SMoTherSpectre: Exploiting speculative execution through port contention*, Bhattacharyya et al., In: ACM Conference on Computer and Communication Security, 2019. (15% acceptance rate).
- *Open Source Cube Satellite Software and Hardware Subsystems*, Stefan E. Damkjar et al., In: 7th European CubeSat Symposium

COURSE PROJECTS

- Advanced Computer Architecture: Implemented an AES accelerator in VHDL achieving a 74x speedup over a software-accelerated version.
- Embedded Systems: Implemented a DMA-enabled controller in VHDL for the TRDB-D5M 5 megapixel camera on an FPGA.
- Real Time Embedded Systems: Implemented an audio capturing and real-time streaming pipeline using an FPGA/Linux.
- Computer Networks: Implemented reliable transport using UDP in Linux.
- Compiler Design: Developed a D to MIPS compiler using Lex/Yacc.
- Computer Architecture: Implemented pipelining in a MIPS simulator in C++.
- Digital VLSI Design: Implemented the layout of a 8-bit bidirectional logarithmic bit-shifter on Mentor Graphics

ACHIEVEMENTS AND AWARDS

2019	3rd	Best Research Presentation Award, IC Research Day, EPFL
2018		EPFL IC School Fellowship
2016		MS Research Scholarship, EPFL
2016	340/340 score	Graduate Record Examinations(GRE)
2014	2^{nd}	UnnaTI intern design contest, Texas Instruments
2014	3^{rd}	Annontrix, Techkriti, IIT Kanpur
2013	2^{nd}	Embedded, Techkriti, IIT Kanpur
2012	2^{nd}	Electromania, Techkriti, IIT Kanpur
2012	University level	Academic Excellence Award for 2011-2012
2011	National level	Indian National Mathematics Olympiad(INMO)
2011	National level	Udhbhav Poddar trophy for ICSE mathematics